

FIG.1

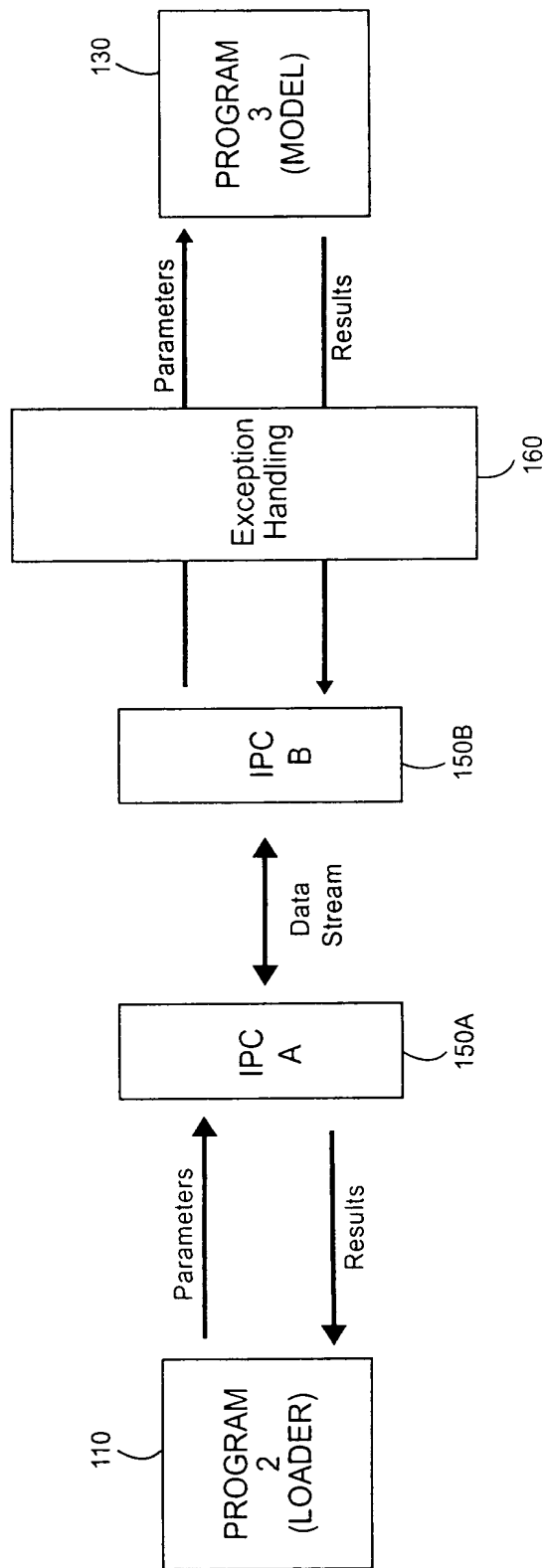


FIG.2

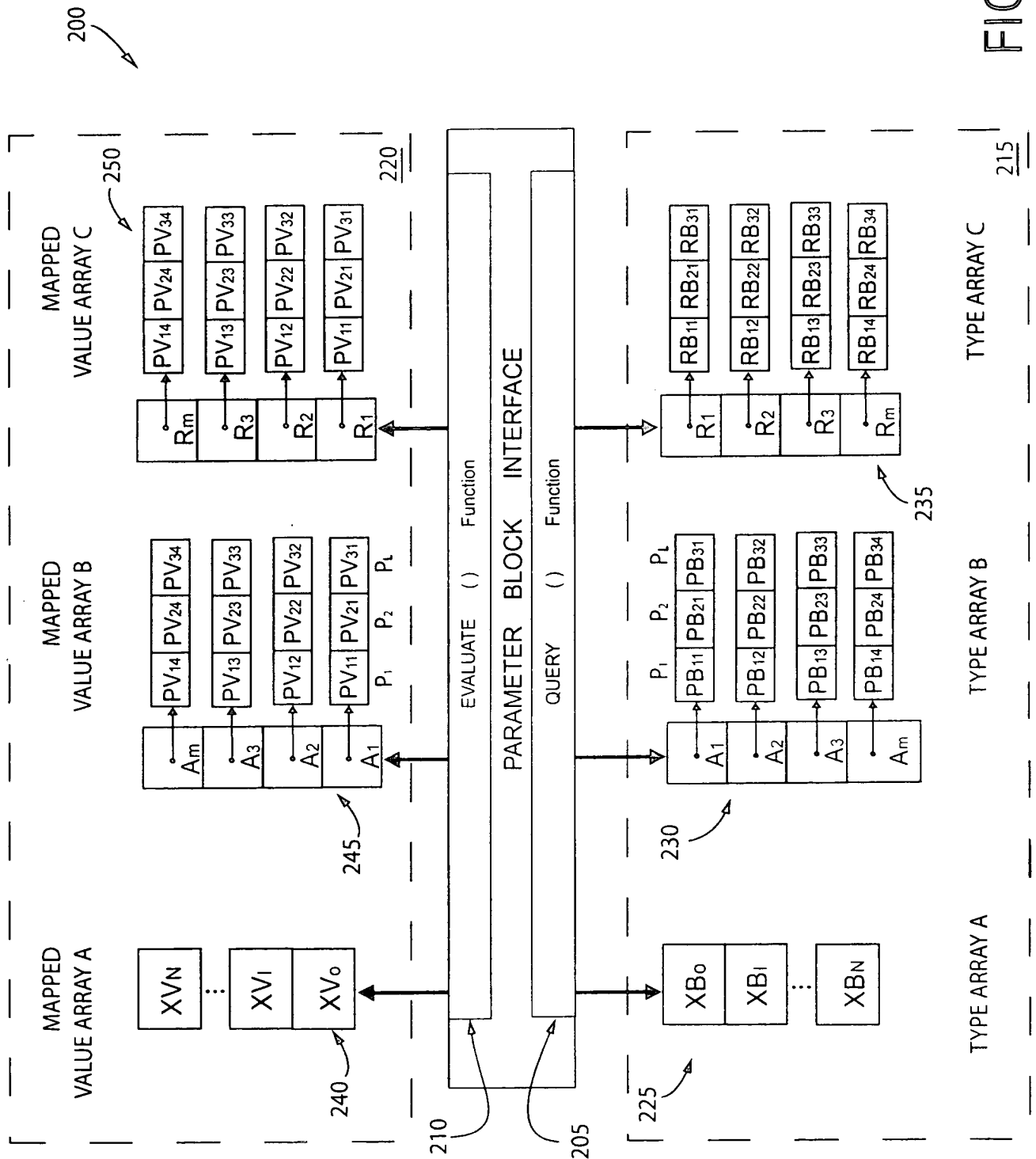


FIG. 3

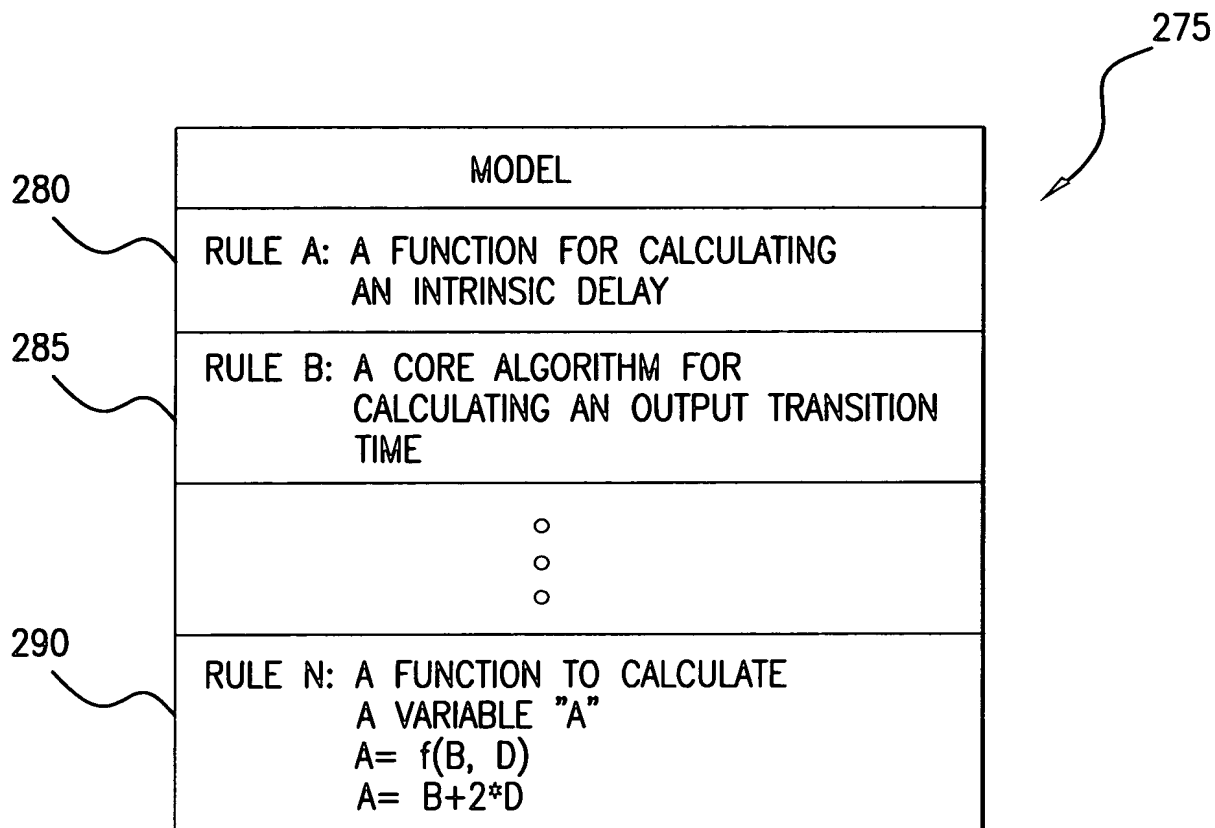


FIG. 4

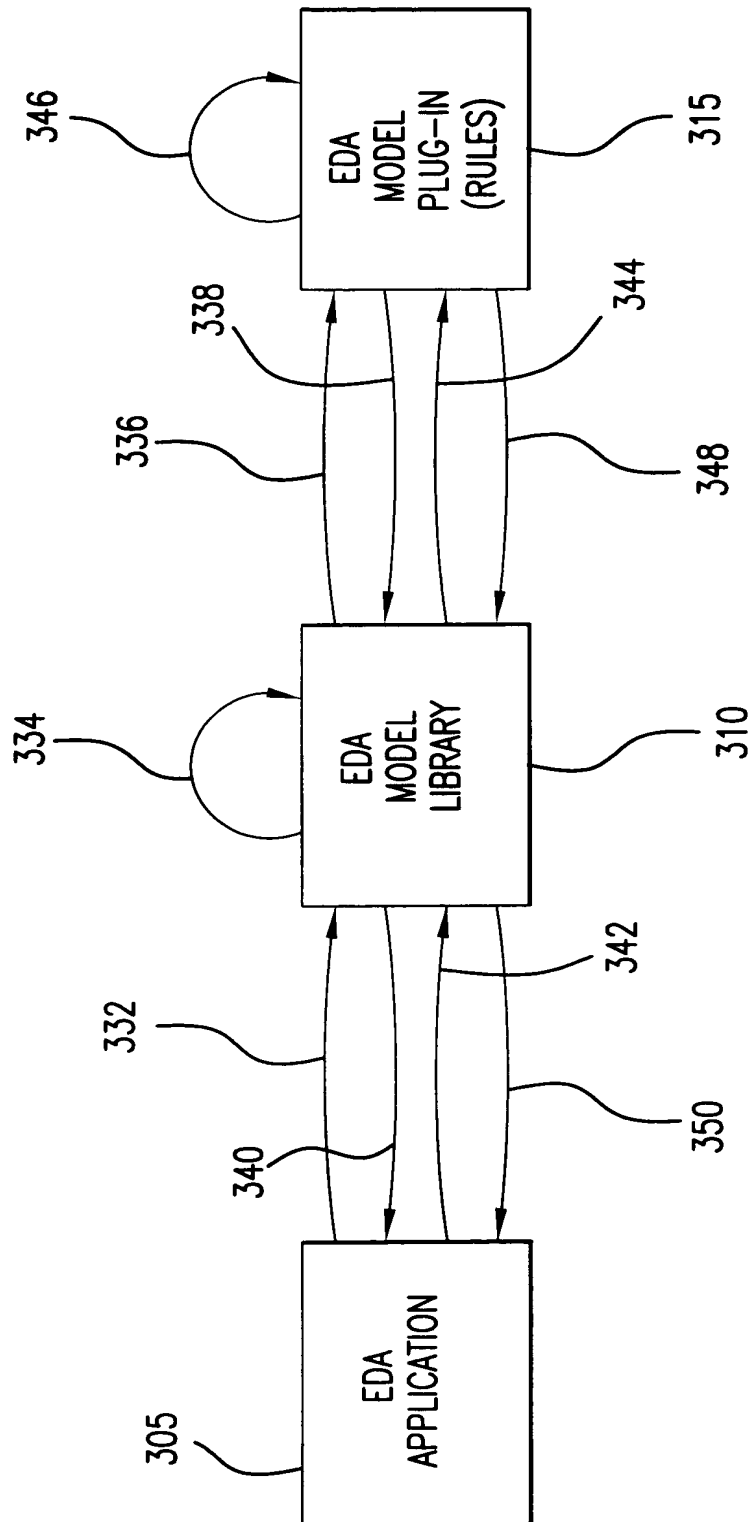


FIG. 5

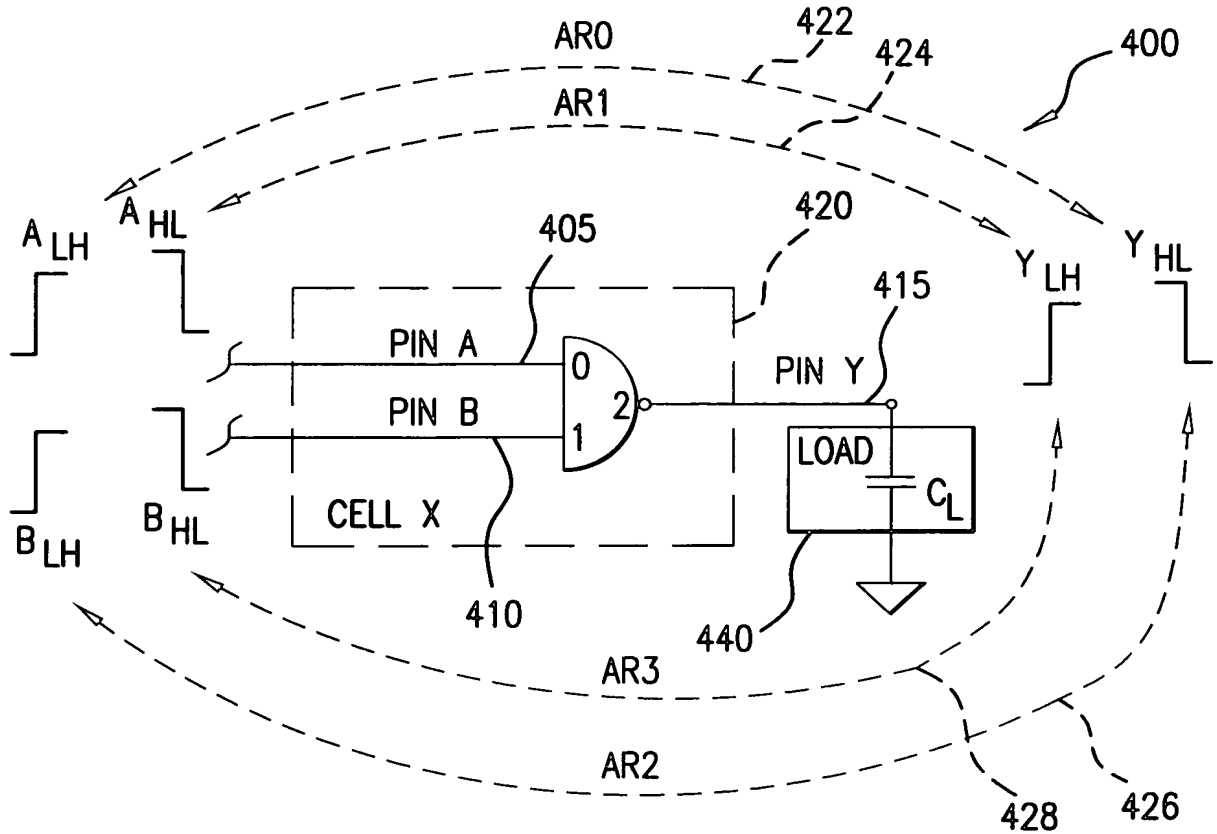


FIG. 6A

ARC RULES	INPUT AT		OUTPUT AT
	PIN A	PIN B	PIN Y
AR0	A <sub>LH</sub>	I	Y <sub>HL</sub>
AR1	A <sub>HL</sub>	I	Y <sub>LH</sub>
AR2	I	B <sub>LH</sub>	Y <sub>HL</sub>
AR3	I	B <sub>HL</sub>	Y <sub>LH</sub>

FIG. 6B

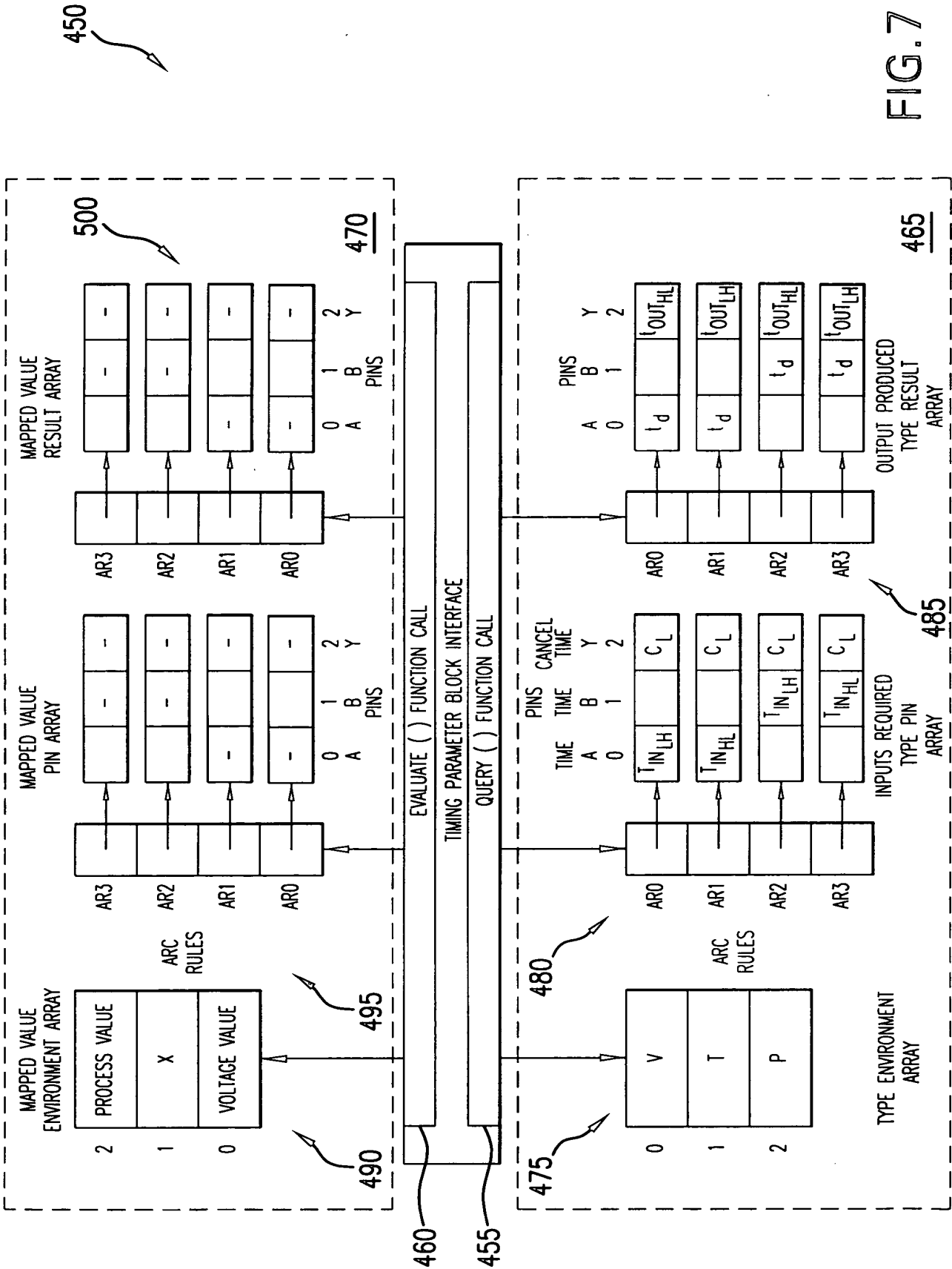


FIG. 7

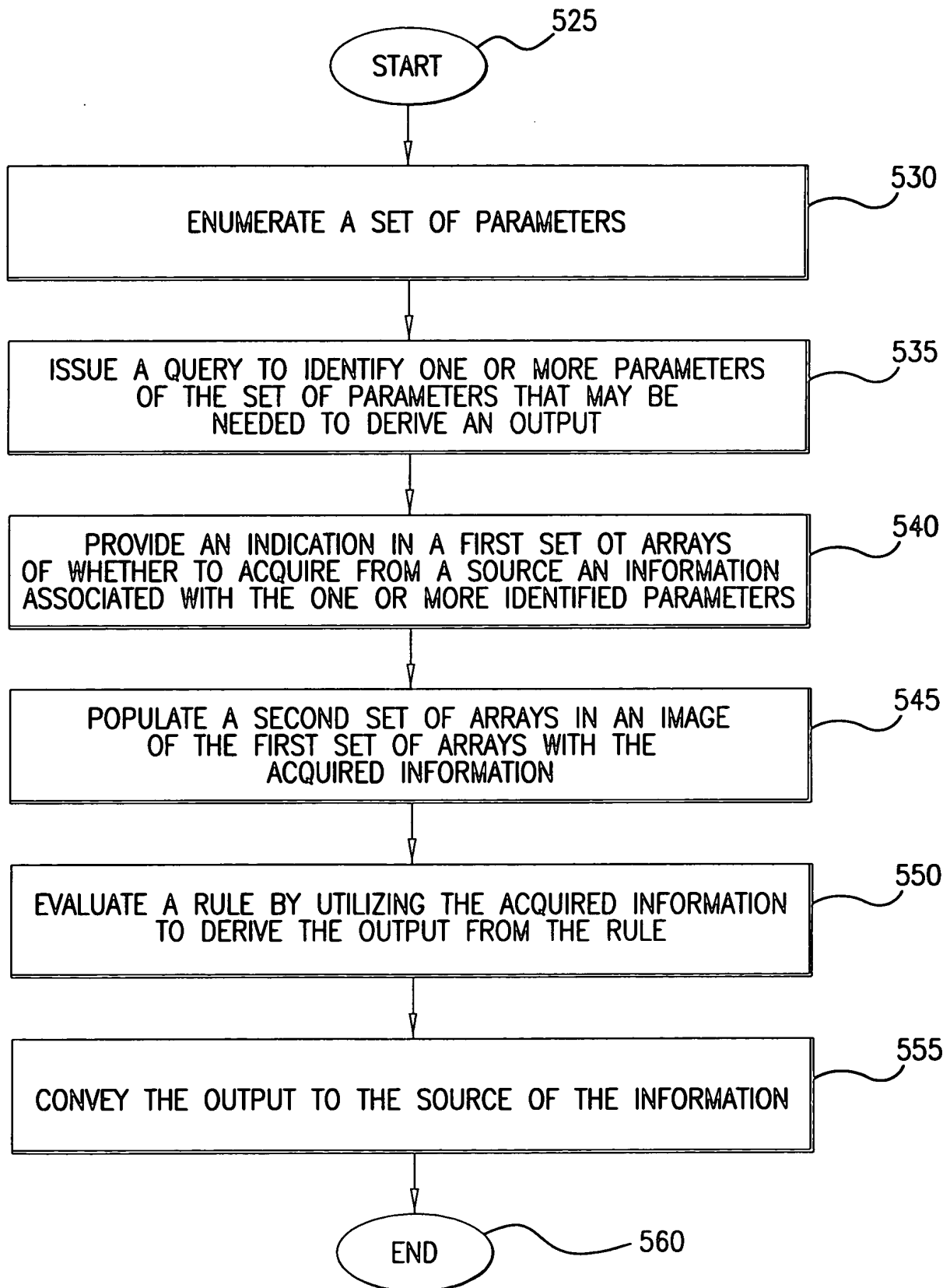


FIG.8A



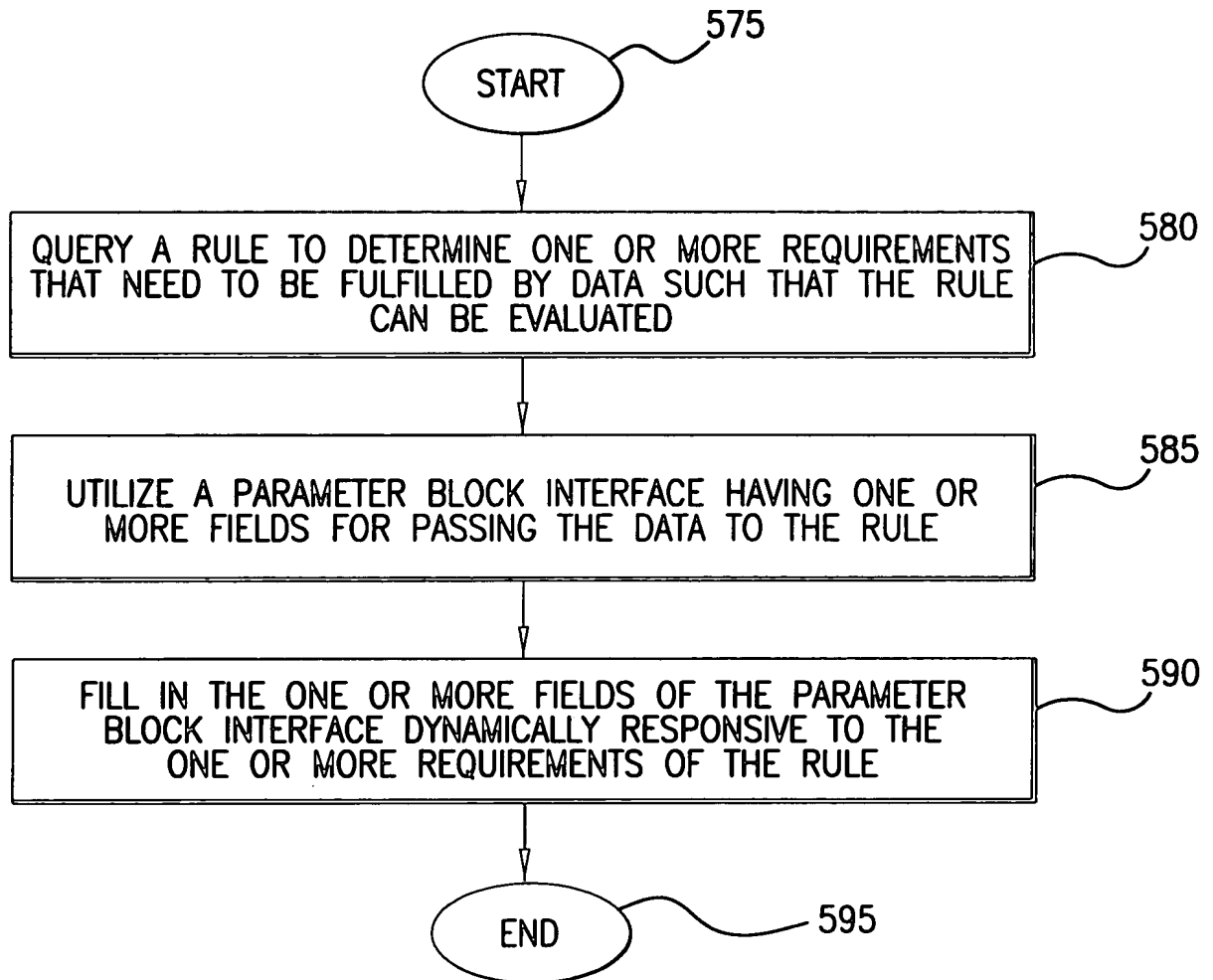


FIG. 8B